ABSTRACT OF THE DISCLOSURE

SYSTEM CHIP SYNTHESIS

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A technique to design deep sub-micron (DSM) integrated circuits is disclosed, in which global wire delays are minimized first, before performing logic synthesis. According to the present method, a designer performs layout of physical blocks by estimating an area for each block. After connecting the pins of the blocks with no timing constraints, each wire is assigned to a metal layer, based on length. The delay of each wire is minimized by inserting buffers at optimal distances. The blocks are then partitioned into "cores" and "shells." The shells and cores are synthesized, and then recombined. This procedure greatly reduces the number of design iterations required to complete a design.